Development of Vertical Interconnect Surface Mount Packages

Hongwei Liang, Carl Chun, Joy Laskar, Don Estriech[1]
School of Electrical and Computer Engineering
Packaging Research Center
Georgia Institute of Technology
Atlanta, GA 30332

[1] Microwave Technology Center
Hewlett-Packard Company
Santa Rosa, CA 95403-1738

Abstract-- A novel vertical interconnect package (VIP) based upon surface mount plastic lead frame packages is presented for microwave applications. The prototype has been fabricated and measured, and its finite element method (FEM) simulation is confirmed by experimental results. This new package demonstrates improvements of approximately 10 dB in return loss and 1 dB in insertion loss over the small shrink outline package (SSOP) to 10 GHz. Investigation into the behavior of the discontinuities has provided insight into mismatches at interconnects, and higher performance prototypes are in fabrication.

I. INTRODUCTION

The rapid growth of the wireless communication market motivates the development of microwave packaging which is a significant portion of the cost in communication systems. Presently low cost plastic surface mount packages are widely used at frequencies below a few GHz. Plastic packages in its current form are limited by parasitic parameters at higher frequencies[1]. Application of a high volume manufacturable technology such as plastic lead frames provides a path for low cost high frequency packages. In this paper, a novel low cost microwave package, the vertical interconnect package (VIP), is introduced. The VIP demonstrates improvement in transmission and reflection loss over SSOPs. A prototype of this package has been measured and simulated.

II. DESCRIPTION OF VERTICAL INTERCONNECT PACKAGE

This paper presents a novel vertical interconnect package utilizing simple fabrication and interconnection techniques. The VIP is a surface mount package with the prototype providing two RF leads and multiple DC connections. Figure 1 shows the top view of a 12-pin VIP before encapsulation. The majority of the frame consists of a ground plane with tabs cut out to provide DC and RF input. The lead frame has a U-shape at each RF port, shielding the signal with the surrounding ground. The chip is mounted in the center of the ground of the lead frame and is connected to signal lines of the lead frame before encapsulation of the package. For our measurement, a 50Ω microstrip through line acts as the packaged component and is wirebonded to the lead frame. The entire package is mounted on an alumina substrate patterned with CPW feeds (shown in Figure 2) for on-wafer probing.

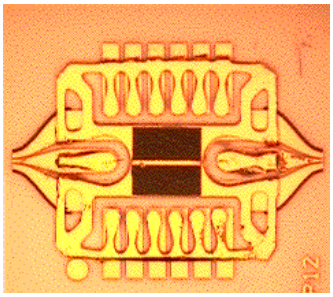

Figure 1: A 12-pin VIP mounted on alumina substrate

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

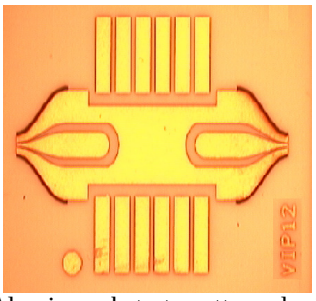

Figure 2: Alumina substrate patterned with CPW feeds

The central concept behind this package is to use a pseudo coaxial feed as a waveguide structure and to minimize the coupling between RF interconnects in the package. To illustrate the improvement, the S-parameters of a VIP and a SSOP package were measured. The two sample packages have similar size and the same number of pins. In Figure 3, we compare measured results of the VIP and SSOP, both with a 50Ω microstrip transmission line mounted on. The measured S-parameters show that the VIP has a return loss better than 12 dB and insertion loss better than 1 dB to 10 GHz. The plot also demonstrates that the VIP has approximately 10 dB better return loss than the SSOP to 10 GHz.

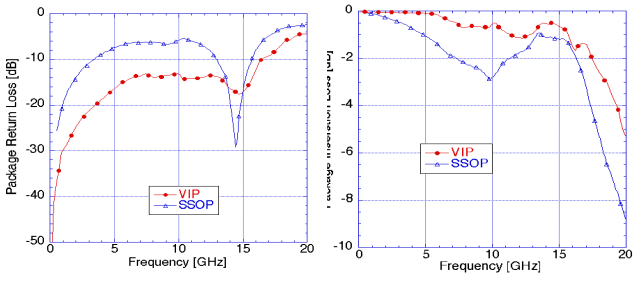

Figure 3: Comparison of S-parameters shows that VIP has a 10dB better return loss and better insertion loss over SSOP at most frequency points below 20GHz.

We have fabricated an 8-pin VIP (VIP8) and a 12-pin VIP (VIP12). The experimental S-parameters are obtained with an HP8510 network analyzer using the LRM (line-reflect-match) calibration technique. We have also simulated the VIP8 using a commercial FEM simulator. The simulated results are in good agreement with experimental data, as shown in Figure 4.

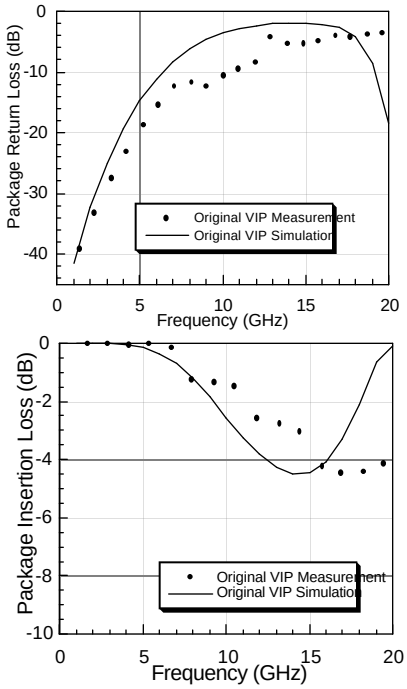

Figure 4: Comparison of FEM simulation result with measurement

III. Study of VIP Electrical Characteristics and Optimization of Structure

Because of the complex multi-material geometrical shapes in the microwave package, many of the recent research on microwave packages relies heavily on various electromagnetic (EM) simulation tools and numerical calculations[2-5]. Our investigation of the first generation VIP combines 3-D FEM simulation, using HFSS, and experimental data. Figure 5 shows the 3D solid model of the VIP for FEM simulation.

The lead frame plays a key role in this package. It provides both a shield for the signal line and an interconnection to the packaged chip. The package can be considered as a sequence of several interconnections, as shown

in Figure 6(a). The discontinuity in the figure is at the interface between the CPW feed and the lead frame. If we consider the lead frame at the discontinuity as a tapered "thick" CPW whose coplanar layer has a height comparable to that of the substrate, the discontinuity then can be characterized as a two port junction of different waveguides, which is illustrated in Figure 6(b). Assuming the difference of wave modes in each waveguide has negligible effect on the packaging performance, we focus on the characteristic impedance (Z_o) of each waveguide. The Z_o of the CPW is 55 Ω, while Z_o of the "thick" CPW is only 40 Ω. Clearly an impedance-mismatch exists at the junction.

In Figure 7, we optimize the geometry of the lead frame in VIP8 using FEM simulation so that the “thick” CPW section has a characteristic impedance of 53Ω to minimize the impedance mismatch. The simulation results are shown in Figure 8. It compares the simulation result of package insertion loss for the original VIP8 and the optimized VIP8 and demonstrates that the resonance has been greatly suppressed.

IV. CONCLUSION

We present in this article a new design for a low cost microwave package. The first measured results of this package demonstrate very good characteristics in the DC to 20 GHz frequency range compared with SSOP packages. FEM simulation and structure analysis have revealed the source of resonance in the prototype VIP, which is greatly suppressed in the optimized structure. A next generation design has been in process of fabrication and a better understanding of this package can be achieved through the problems revealed by simulation and experiment. The results presented here demonstrate that the VIP provides the possibility for low-cost millimeter-wave surface mount plastic packages.

Acknowledgements

This work was supported by NSF CAREER Award under contract ECS-9623964 and NSF Packaging Research Center at Georgia Tech under contract ECS-9402723. The authors would like to thank Larry McBride and Brian Hutchison at Hewlett-Packard for their valuable help.

REFERENCES

[1] C.Chun, A.Pham, J.Laskar, B.Hutchison, "Development of Microwave Package Models Utilizing On-Wafer Characterization Techniques", *IEEE Trans. Microwave Theory Tech*, pp.1948-1954, Vol. 45, No 10, Oct 1997

[2] J.Yook, L.Katehi, R.Simons, K.Shalkhauser, "Experimental and Theoretical Study of Parasitic Leakage/Resonance in a K/KA-Band MMIC Package", *IEEE Trans. Microwave Theory Tech*, pp.2403-2410, Vol. 44, No 12, Dec 1996

[3] B.Spielman and L.Chen, "A Full-Wave Analysis for Microwave, Planar, Distributed Discontinuities", *IEEE MTT-S Digest*, 1996, pp1055-1058

[4] F.Alimenti, P.Mezzanotte, L.Roselli, "Full-Wave Investigation on the Curved Bonding Wire Interconnection by using a Suitable FDTD Code", *IEEE MTT-S Digest*, 1997, pp1737-1740

[5] Hai-Young Lee, "Wideband Characterization of a Typical Bonding Wire for Microwave and Millimeter-wave Integrated Circuits", *IEEE Trans. Microwave Theory Tech*, pp.63-68, Vol. 43, No 1, Jan 1995

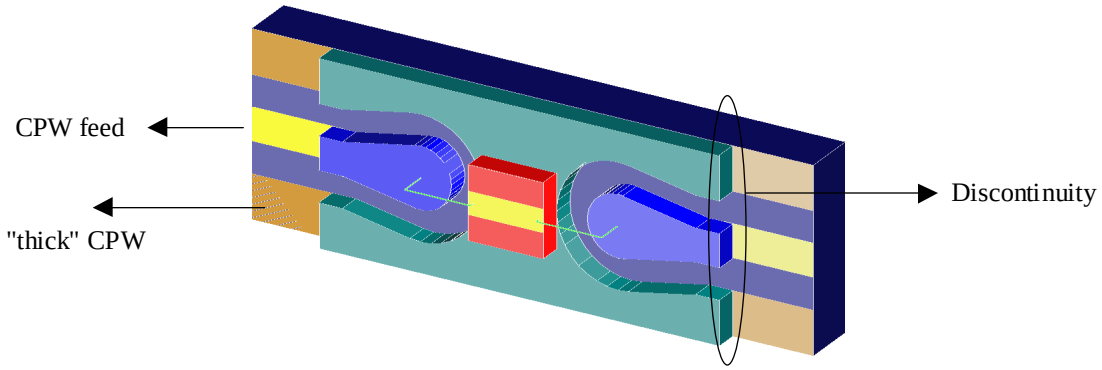

Figure 5: 3-D simulation model of first generation VIP

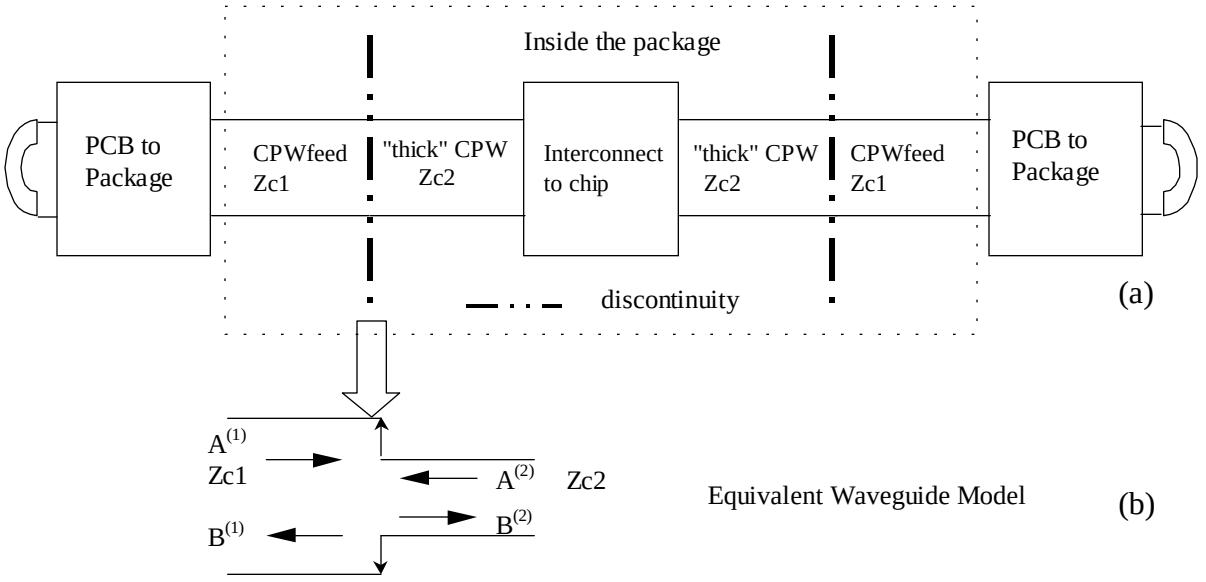

Figure 6: (a)Schematic Circuit model of VIP.
(b)The discontinuity is modeled as a junction of two transmission lines with different characteristic impedance.

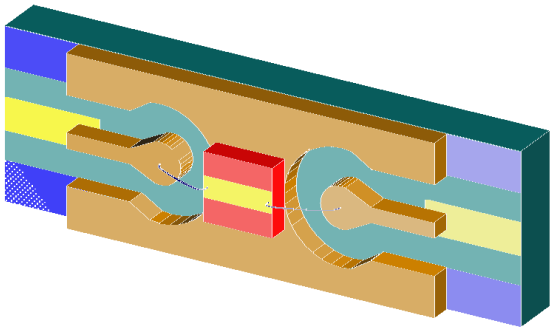

Figure 7: 3-D simulation model for redesigned VIP

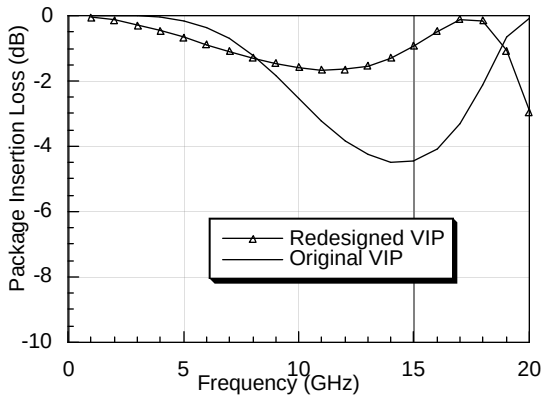

Figure 8: Comparison of FEM simulation of redesigned VIP and original VIP